IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	Civil Action No.:1:19-cv-00977-ADA

DEFENDANT INTEL CORPORATION'S
RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

As Intel correctly predicted, the parties' opening briefs reflect vastly different approaches to claim construction. For each term, Intel's brief identifies the specific meaning the term should have, backed by a detailed explanation as to why the controlling intrinsic evidence requires that construction. By contrast, for most terms, VLSI does not even say in its brief what it believes the term should mean—beyond generic labels such as "plain and ordinary meaning" and "definite." And even when purporting to discuss the intrinsic evidence, VLSI entirely ignores the most relevant disclosures in the patent and prosecution history—in which the patentees expressly defined the scope of the alleged inventions and specific terms in dispute here, including via clear descriptions of "the present invention" and disclaimers made to avoid invalidating prior art.

That VLSI feels compelled to resort to these improper and unfair "hide-the-ball" tactics only further underscores the merits of Intel's proposed constructions. It also affirms more broadly that constructions of these terms are needed to prevent VLSI from shielding its true positions until trial, and then arguing to the jury that the terms cover things the asserted patents do not purport to invent and/or that were previously disclaimed to obtain issuance of the asserted claims in the first instance. Accordingly, for the reasons set forth below and in Intel's opening brief, Intel's proposed constructions should be adopted.

II. U.S. PATENT NO. 6,366,522

A. Disputed Term: "regulate [regulating] at least one supply from a power source and an inductance" (all claims)

Intel's Construction	VLSI's Construction
Regulate [regulating] at least one supply from an inductance connected to a power source, where the inductance is positioned between the power source and the regulating circuitry	Plain and ordinary meaning

In its opening brief, Intel explained in detail how, during reexamination before the Patent

Office, the patentee (successfully) distinguished the '522 patent from eight different prior art references that disclose buck regulators—by clearly and repeatedly characterizing this limitation as requiring "an inductance" that is both (1) connected to the power source and (2) positioned between the power source and regulating circuitry, just as Intel has proposed here. Intel Br. at 3-7. VLSI's brief raises several arguments in response, none of which has merit.

First, VLSI states that Intel's construction "appears to conjure this limitation from thin air." VLSI Br. at 6. But as noted above and in Intel's opening brief, Intel's construction comes ***directly*** from the reexamination history—in which the patentee overcame multiple prior art rejections only by disclaiming buck regulator configurations in which an inductance is ***not connected*** to the power source and ***does not sit between*** the power source and regulating circuitry. Intel Br. at 3-7 (explaining how, in a buck regulator configuration, an inductance instead appears ***after*** the regulating circuitry and is used to smooth the output of that circuitry); DX-6 [Apsel Decl.] ¶¶ 31-50. VLSI tellingly fails to even mention the reexamination history of its own patent—presumably because it knows that disclosure is fatal to its position.

Second, VLSI maintains that "Intel's construction provides no insight into what it means to 'regulate at least one supply from a power source and an inductance.'" VLSI Br. at 6. Not so. Again, Intel has proposed the precise meaning that the patentee attributed to that claim language during reexamination. By contrast, VLSI argues that no construction is required and that "this term should … be given its plain and ordinary meaning"—without ever hinting at what that supposed meaning might be. *Id.* at 5. The reason for that silence is simple: at trial, VLSI presumably wants to argue that the asserted claims cover the very type of buck regulator that the patentee was forced to disclaim during reexamination. Intel's proposed construction is required to prevent VLSI from unfairly doing so. *See NobelBiz, Inc. v. LiveVox, Inc.*, 2015 WL 225223, at

*13 (N.D. Cal. Jan. 16, 2015) (criticizing argument "that plain and ordinary meaning should apply [that] fails to identify what that meaning is"); *Datatreasury Corp. v. Wells Fargo & Co.*, 2009 WL 1393068, at *65 (E.D. Tex. May 11, 2009) (rejecting plaintiff's argument for "plain and ordinary meaning" construction that "fails to explain (1) what the plain and ordinary meaning is and (2) how Defendants' proffered construction is different from the plain and ordinary meaning"); *see also Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1375 (Fed. Cir. 2008) ("Claims should not be construed 'one way in order to obtain their allowance and in a different way against accused infringers.'" (citation omitted)).

Third, VLSI contends that Intel's construction "violates black letter law on importing limitations from the specification." VLSI Br. at 6. Once again, however, Intel's construction comes directly from the express representations about claim scope made during reexamination—and not merely because the patent discloses an embodiment consistent with Intel's construction.[1]

Nor can VLSI override that express prosecution history disclaimer merely by citing to the specification's generic statement that "other embodiments" are possible. *See Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325-27 (Fed. Cir. 2002) (holding that prosecution history disclaimer supported construction that excluded preferred embodiment); *nCAP Licensing, LLC v. Apple Inc.*, 2019 WL 2409666, at *6 (D. Utah 2019) ("When a patentee has disavowed a claim scope that would cover embodiments disclosed in the specification, there is no legal requirement the disavowed claim be construed to embrace such embodiments.").

Finally, VLSI argues that Intel's proposed construction should be rejected under the

[1] VLSI implicitly admits that, consistent with Intel's construction, the specification describes a boost regulator that regulates at least one supply from an inductance connected to a power source, where the inductance sits between the power source and regulating circuitry. *Id.* ("Intel's proposal ... import[s] limitations from the specification.").

doctrine of claim differentiation—because claim 1 requires "an inductance," while dependent claim 25 specifies "wherein the inductance is an external inductance." VLSI Br. at 6. But the mere fact that an inductance can be "external" to a chip is not inconsistent with Intel's construction; indeed, the '522 patent itself shows an "external" inductance that is (1) connected to a power source and (2) sits between the power source and regulating circuitry. DX-1 ['522 patent], 2:29-34, Fig. 1 (showing "external inductor 60" connected to power source 62 and located between power source 62 and regulating circuitry comprising transistors 48 and 50). Moreover, claim differentiation is inapplicable where, as here, a party seeks to use that doctrine to re-capture disclaimed claim scope. *See Seachange Int'l, Inc. v. C–COR, Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005) (claim differentiation is "not a hard and fast rule and will be overcome by a contrary construction dictated by the written description or prosecution history").

Accordingly, because Intel's construction captures the precise meaning that the patentee applied during reexamination to distinguish the prior art, that same meaning should be adopted here.

III. U.S. PATENT NO. 7,292,485

A. Disputed Term: "a capacitance structure" (claims 1, 12, 17)

Intel's Construction	VLSI's Construction
Function: providing "capacitance" **Structure**: (1) Dummy column 17 (comprised of dummy SRAM cells 30, 32, and 34 and dummy bitlines SBL and SBL*) and conductor 37, configured to be selectively coupled to one or more of the dummy SRAM cells, as shown in Figure 2, and equivalents thereof; or alternatively (2) dummy row 70 (comprised of dummy SRAM cells 82, 84, and 86 and dummy wordline SWL) and conductor 71, configured to be selectively coupled to one or more dummy of the SRAM cells, as shown in Figure 3, and equivalents thereof	Plain meaning; not means-plus-function

As Intel's opening brief demonstrated, "capacitance structure" is a purely functional term

that does not connote any definite structure, and therefore is a means-plus-function limitation under 35 U.S.C. §112, ¶ 6 (that has the claimed function and structure that Intel has proposed). Intel Br. at 9-12. In response, VLSI does not contest Intel's identification of the corresponding structure that the patent discloses for performing the function of providing capacitance. As such, to the extent the Court agrees with Intel that "capacitance structure" is a means-plus-function limitation, Intel's proposed structure should be adopted as undisputed.

VLSI instead raises a host of flawed arguments in an attempt to avoid having "capacitance structure" treated as a means-plus-function limitation at all, each of which fails.[2]

First, VLSI relies on the fact that the claim term does not include the word "means." VLSI Br. at 8. But as the *en banc* Federal Circuit confirmed in *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (*en banc*) (quoting *Watts v. XL Sys., Inc.*, 232 F.3d 877, 880 (Fed. Cir. 2000)), a claim term that "fails to 'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function'" is a means-plus-function term—***regardless*** of whether the term uses "means" (or not). For that reason, courts have regularly interpreted limitations missing the word "means" as means-plus-function terms—including those, like here, that involve nonce words such as "structure." Intel Br. at 10-11. *E.g.*, *Grecia v. Samsung Elecs. Am., Inc.*, 780 F. App'x 912, 914-17 (Fed. Cir. 2019) ("customization module" construed as means-plus-function term); *Advanced Ground Info. Sys., Inc. v. Life360, Inc.*, 830 F.3d 1341, 1347 (Fed. Cir. 2016) ("symbol generator" construed as means-plus-function term); *Scarborough v. Integricert, LLC*, 2015 WL 5099128, at *13 (W.D. La. Aug. 31, 2015) ("attachment structure" construed as mean-plus function term); *In re Katz Interactive Call*

[2] Nor does VLSI attempt to defend its own "plain meaning" construction; VLSI alleges that the term has a "plain meaning," but nowhere explains with any clarity what that plain meaning is.

Processing Patent Litig., 2008 WL 4865032, at *13 (C.D. Cal. Mar. 4, 2008) ("gang holding structure" construed as means-plus-function term).[3]

Second, VLSI attempts to avoid the patent's functional claiming by urging that an artificial distinction exists between the "physical properties" of a structure and its "functions." This argument finds no support in the law or the art. Indeed, both parties' experts agree that "capacitance" refers to the ***ability*** to perform the ***function*** of storing electric charge. DX-6 [Apsel Decl.] ¶ 58 ("The ***ability to store a charge*** is known as capacitance."); Dkt. No. 81-1 [Conte Decl.] ¶ 15 ("[Capacitance] refers to the ***capability*** of a physical structure, or system, ***to hold electric charge***."); *see* DX-27 [*Academic Press Dictionary of Sci. and Tech.*] at 353 (defining "capacitance" as "the ***ability*** … ***to store energy in the form of electrically separated charge***"); DX-28 [*Wiley Elec. and Elecs. Eng'g Dictionary*] at 92 (defining "capacitance" as "[t]he ***ability to store electric charge*** between conductors which are separated by a dielectric material"); DX-29 [*Am. Heritage Sci. Dictionary*] at 97 (defining "capacitance as "[a] measure of the ***ability*** of a configuration of materials ***to store electric charge***").

Because the claimed "capacitance structure" is a generic "structure" characterized solely by its ability to perform the function of storing charge, it is a functional term, not a structural one. *See Nichia Corp. v. TCL Multimedia Tech. Holdings, Ltd.*, 2017 WL 5719267, at *8-9 (D. Del. Nov. 28, 2017) (construing "reflective member" and "dispersive member" as means-plus-function limitations because the ability to reflect light and disperse light were functions).

Further, VLSI's own cited examples of purportedly comparable "properties" serve only to

[3] VLSI relies entirely on pre-*Williamson* cases, which applied a "strong" presumption that terms lacking the word "means" were not means-plus-function. VLSI Br. at 10-11 (citing cases before *Williamson* issued in 2015). The *en banc* Federal Circuit expressly abandoned this standard in *Williamson*, "overrul[ing] the strict requirement of 'a showing that the limitation essentially is devoid of anything that can be construed as structure.'" *Williamson*, 792 F.3d at 1349.

confirm the functional nature of the term. VLSI argues that "capacitance" is "like temperature, mass, or resistance." VLSI Br. at 8. But it does not even attempt to explain how a "temperature structure," "mass structure," or "resistance structure" would connote any definite structure either. Instead, like the claimed "capacitance structure," each of those terms would be defined only by the functions they perform, and thus would be means-plus-function limitations as well.[4]

Third, VLSI contends that a skilled artisan would have understood that "capacitance structure" refers to a "well-known class of physical structures." VLSI Br. at 9. But VLSI tellingly fails to identify a single treatise, publication, or other reference defining this purportedly well-known class of structures. The reason for this lack of evidence is plain: contrary to VLSI's bare attorney assertions, the term "capacitance structure" has no well-understood structure, including in the specific context of dummy cells.

In fact, VLSI's expert Dr. Conte states only that a "capacitance structure" would encompass structures that "have capacitance." Dkt. No. 81-1 [Conte Decl.] ¶ 14. But that proves Intel's point that the term "capacitance structure" is defined only by the function performed (i.e., providing capacitance). Moreover, if accepted, Dr. Conte's definition would render the claim term "capacitance" meaningless because (1) as Dr. Apsel has explained, virtually ***every*** integrated circuit component "has capacitance," and (2) VLSI and Dr. Conte fail to provide any guidelines or other boundaries that would allow persons of ordinary skill to assess with any reasonable

[4] VLSI's reliance on *Skky, Inc. v. MindGeek, s.a.r.l.*, 859 F.3d 1014 (Fed. Cir. 2017), is similarly misplaced. In that case, the Federal Circuit recognized that the disputed term had an established meaning "in common parlance." *Id.* at 1020. And because that known meaning designated structure, the term sufficiently recited a particular structure. *Id.* Here, in contrast, VLSI has presented ***no evidence*** "in the form of dictionary definitions or otherwise" that "capacitance structure" refers to a definite structure. *See Diebold Nixdorf, Inc. v. ITC*, 899 F.3d 1291, 1302 (Fed. Cir. 2018) (holding *Skky* did ***not*** apply because, despite expert's testimony that term had a structural meaning, there was no evidence "that 'cheque standby unit' was reasonably well understood by persons of ordinary skill in the art to refer to a structure or class of structures").

certainty which of these structures fall within VLSI's supposed class of structures covered by the claims and which ones do not. DX-6 [Apsel Decl.] ¶ 58; *e.g.*, DX-29 [*Am. Heritage Sci. Dictionary*] at 97 ("Most electrical components display capacitance to some degree; even the spaces between components of a circuit have a natural capacitance.").[5]

Fourth, VLSI argues that Intel's construction would improperly render other structural aspects of the claims—directed to a "dummy line" and "plurality of dummy cells"—superfluous. VLSI Br. at 10. As an initial matter, the preference for avoiding superfluous claim language "is not an inflexible rule," particularly for means-plus-function terms. *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 429 (Fed. Cir. 2016); *see Laitram Corp. v. Rexnord, Inc.*, 939 F.2d 1533, 1538 (Fed. Cir. 1991) (holding "judicially developed guide[s] to claim interpretation" cannot "override" the statutory language of Section 112, ¶ 6). And in any event, Intel's proposed construction does not render any limitations superfluous. To the contrary, the claim language that VLSI cites imposes additional restrictions on those structures. *K2M, Inc. v. OrthoPediatrics Corp.*, 2018 WL 2426660, at *1 n.7 (D. Del. May 30, 2018) (rejecting argument that corresponding structure of means-plus-function term cannot include structure expressly recited elsewhere in the claim).

For example, consistent with the corresponding structure disclosed in the specification, Intel's construction includes a column or row of dummy cells and a conductor (37 or 71) that can

[5] Even under VLSI's interpretation the claims are indefinite because the term "capacitance structure" is not reasonably clear as to what level of capacitance would be required, and neither the specification nor the prosecution history provides any further guidance. DX-31 [Apsel Suppl. Decl.] ¶ 5. *See Berkheimer v. HP Inc.*, 881 F.3d 1360, 1363-64 (Fed. Cir. 2018) (failure to provide an "objective boundar[y]" for term "minimal redundancy" rendered claim indefinite). If VLSI contends that "capacitance structure" encompasses any circuit structure that has capacitance, the claims would "in effect claim[] everything that [performs the function] under the sun" and "are therefore indefinite …." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 519 (Fed. Cir. 2012).

be ***selectively coupled*** to any ***one or more*** of the dummy cells, and ***equivalents*** thereof. DX-2 ['485 patent], 4:44-46 ("The capacitance of dummy column 17 can be adjusted by selecting the number of memory cells coupled to conductor 37); *id.*, 6:27-32 (similar). The added requirement in claims 1 and 12 for "a ***plurality*** of dummy cells" merely means that the claims have a narrower scope than they would if they merely recited a "capacitance structure." Specifically, this reference confirms that the capacitance structure must include a plurality of dummy cells—rather than the broader structural "equivalents thereof" that would otherwise be captured by Intel's construction (below) and by Section 112, ¶ 6:

> (1) Dummy column 17 (comprised of dummy SRAM cells 30, 32, and 34 and dummy bitlines SBL and SBL*) and conductor 37, configured to be selectively coupled to one or more of the dummy SRAM cells, as shown in Figure 2, ~~and equivalents thereof~~; or alternatively (2) dummy row 70 (comprised of dummy SRAM cells 82, 84, and 86 and dummy wordline SWL) and conductor 71, configured to be selectively coupled to one or more dummy of the SRAM cells, as shown in Figure 3, ~~and equivalents thereof~~

See Williamson, 792 F.3d at 1347 (explaining how means-plus-function claiming "restrict[s] the scope of coverage to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof"); *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1431 (Fed. Cir. 2000) ("The scope of claim 3 is clearly narrower than that of claim 1 because claim 3 covers only a tape cassette transport, whereas claim 1 covers a tape cassette transport and its equivalents in accordance with § 112, ¶ 6.").[6]

Likewise, dependent claims 3 and 19 further limit the claims by specifying ***which*** dummy cells are coupled to the conductor (the "dummy line")—in claim 3, "the ***plurality*** of dummy cells" referenced in claim 1 is coupled to the dummy line, while in claim 19, a plurality of dummy cells

[6] The specific reference to a plurality of dummy cells in claim 1 also provides an antecedent basis for the recitation of "***the*** plurality of dummy cells" in dependent claim 3.

is coupled to a dummy line, and ***one*** dummy cell is ***not*** coupled to the dummy line. These additional requirements are consistent with Intel's proposed structure and the specification figures and text (which disclose that the capacitance of the dummy column or line can be adjusted by adjusting the number of dummy cells coupled to the dummy line). For example, as depicted below, Figure 2 (like claims 3 and 19) shows a plurality of dummy cells coupled to the dummy line, and (like claim 19) one dummy cell not coupled to the dummy line:

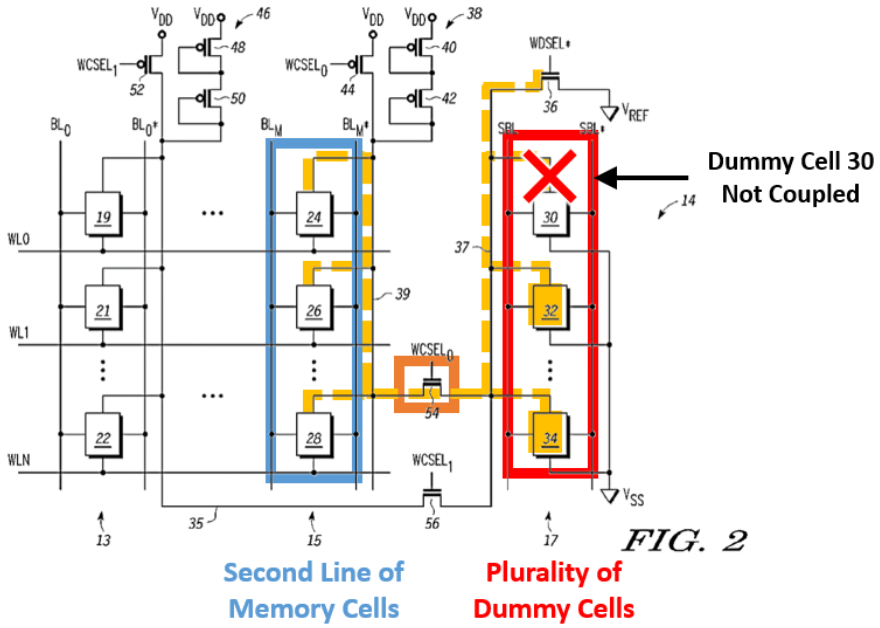

FIG. 2

DX-2 ['485 patent], Fig. 2, 4:46-50.[7]

In sum, VLSI cannot avoid a means-plus-function construction simply because other claim limitations impose ***additional*** restrictions for the structure required by the "capacitance structure" element. *See Transocean Offshore Deepwater Drilling, Inc. v. Pac. Drilling, Inc.*, 2015 WL 3422410, at *31 n.21 (S.D. Tex. May 27, 2015) (language that results in dependent claim having a narrower scope than the claim from which it depends is not superfluous). DX-31 [Apsel Suppl.

[7] Figures 2 and 3, for example, show only two of the three dummy cells (32 & 34 and 84 & 86) coupled to the power line (illustrated with an X showing that the third dummy cell is uncoupled). *Id.*, 4:46-50, 6:27-32.

Decl.] ¶ 6.

Finally, VLSI asserts that the claimed "capacitance structure" is structural because the claims describe it as coupled to and interacting with other physical structures. VLSI Br. at 10. The Federal Circuit has held, however, that merely reciting a component's location in the claimed invention does ***not*** confer structure. *Diebold Nixdorf*, 899 F.3d at 1298 (construing limitation as means-plus function even where the "claims describe[d] the term 'cheque standby unit' solely in relation to its function ***and location in the apparatus***"). This is particularly true for claim 17 of the '485 patent, where even terms that VLSI ***agrees*** are means-plus-function—the "coupling" and "decoupling" means—describe physical couplings between components. DX-31 [Apsel Suppl. Decl.] ¶ 7.

Accordingly, applying the proper legal standard, "capacitance structure" is a means-plus-function limitation with the corresponding structure that Intel has identified.

B. Disputed Term: "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" (claim 17)

Intel's Construction	VLSI's Construction
Function: "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" **Structure**: (1) voltage source V_{REF} and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2, and equivalents thereof; or alternatively (2) voltage source V_{REF} and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3, and equivalents thereof	**Function**: "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" **Structure**: "a conductor, or equivalents thereof"

As Intel's opening brief demonstrated, the '485 specification describes the claimed "precharging" function as performed by: (1) a voltage source that provides the reference voltage (V_{REF}) for the precharging; (2) a conductor (37 or 71) that carries the reference voltage to the

dummy cells; and (3) a transistor (36 or 90) that couples the voltage source to the conductor. As such, Intel's proposed corresponding structure should be adopted. Intel Br. at 13-14.

By contrast, VLSI focuses ***solely*** on the conductor, and attempts to dismiss the other required voltage source and transistor structures as merely "enabling" precharging. VLSI Br. at 11-15. But the specification confirms that the function of "precharging" the capacitance structure requires providing a predetermined voltage to a column or row of dummy cells. DX-2 ['485 patent], 4:30-34 ("Reference voltage V_{REF} is provided to the supply terminals of memory cells 30, 32, and 34 precharging the cells of dummy column 17 to V_{REF} (ground)."); *id.*, 6:14-16 (same for Fig. 3). The specification also clearly links the precharging function to the collective structure of "conductor 37 … coupled to receive a reference voltage labeled 'V_{REF}' via an N-channel transistor 36." *Id.*, 4:7-14, 4:28-33, 5:61-64, 6:11-16 (similar disclosure for Fig. 3).

Moreover, VLSI has not explained how a conductor, by itself, could perform the claimed "precharging" function—because it cannot. Indeed, the specification itself confirms that a voltage source is required to provide the reference voltage (V_{REF}). *Id.*, 4:30-33; 6:13-16. The specification also confirms that a transistor (36 or 90) is needed to control when the conductor (37 or 71) is coupled to the reference voltage. *Id.*, 4:7-8, 5:57-59. In fact, without the transistor, the conductor would ***always*** be connected to the reference voltage, and the voltage of the dummy cells would be fixed at that reference voltage—thereby defeating the intended purpose of the alleged invention. DX-31 [Apsel Suppl. Decl.] ¶¶ 10-11. Accordingly, the voltage source and transistors that Intel has identified are necessary parts of the corresponding structure, and thus should be adopted.

C. Disputed Term: "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" / "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" (claim 17)

'485 Patent Term	Intel's Construction	VLSI's Construction
"first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" (claim 17)	**Function**: "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" **Structure**: (1) transistor 52 and clamping circuit 46, configured to couple power supply voltage V_{DD} and conductor 35, as shown in Figure 2 (if the second line of memory cells is SRAM column 15), and equivalents thereof ; or alternatively (2) transistor 96 and a clamping circuit, configured to couple power supply voltage V_{DD} and conductor 67, as shown in Figure 3 (if the second line of memory cells is SRAM row 68), and equivalents thereof	**Function**: "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" **Structure**: "a switching circuit, or equivalents thereof"
"second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" (claim 17)	**Function**: "coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" **Structure**: (1) Transistor 54, configured to couple conductor 39 to conductor 37, as shown in Figure 2 (if the second line of memory cells is SRAM column 15); or alternatively (2) transistor 94, configured to couple conductor 69 to conductor 71, as shown in Figure 3 (if the second line of memory cells is SRAM row 68)	**Function**: "coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" **Structure**: "a switching circuit, or equivalents thereof"

As the '485 claim language confirms, the "first coupling means" must perform the function of coupling the ***first*** power supply line (supplying the ***first*** line of memory cells) to the power supply terminal during a write operation to the second line of memory cells—so the first line of memory cells continues to receive the power supply voltage. Meanwhile, the "second coupling means" must perform the function of coupling the ***second*** supply line (supplying the ***second*** line of memory cells) to the capacitance structure during the same write operation to the second line of memory cells—to reduce the voltage supplied to the second line of memory cells during the write operation to those cells. Intel's proposed constructions faithfully identify the components in the specification that perform these functions (depicted below), as Intel has previously explained:

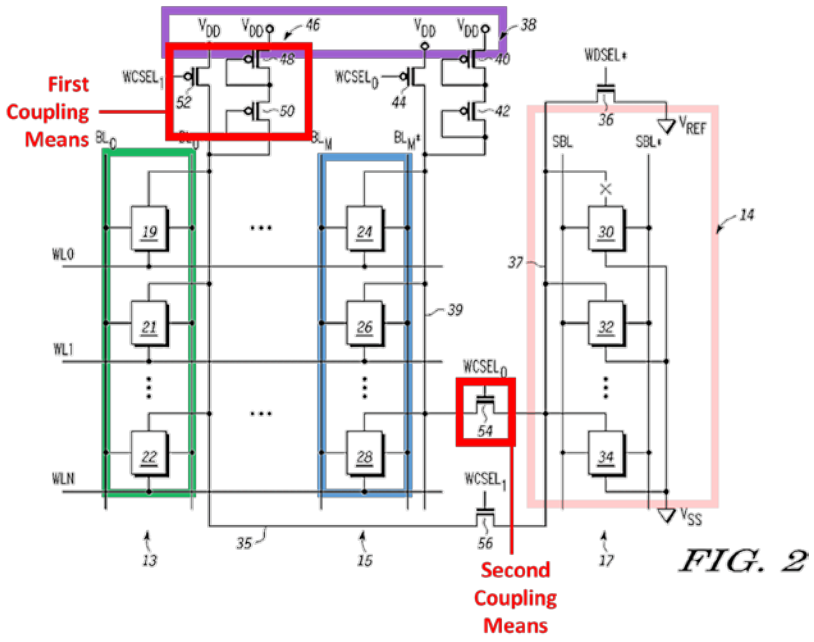

FIG. 2

Intel Br. at 15-17.

In its brief (and constructions), VLSI makes no attempt to identify the structures that perform these different functions. Instead, VLSI simply proposes the same generic structure—a "switching circuit"—for both coupling means. As discussed below, VLSI's construction is not supported by the specification and should be rejected.

1. The Specification Does Not Support VLSI's Proposed Construction of a "Switching Circuit."

For its proposed structure, VLSI identifies a single paragraph in the specification (and a similar statement in the abstract) that merely paraphrases the claim language of claim 1:

VLSI's Cited Portion of Specification	'485 Claim 1
Generally, in one embodiment, a memory circuit comprises a memory array having a first line of memory cells, a second line of memory cells, a first power supply terminal, and a first capacitance structure. A first power supply line is coupled to the first line of memory cells. A second power supply line is coupled to the second line of memory cells. A switching circuit that has	A memory circuit, comprising: a memory array comprising a first line of memory cells and a second line of memory cells; a first power supply terminal; a first capacitance structure includes a plurality of dummy cells; a first power supply line coupled to the first line of memory cells;

VLSI's Cited Portion of Specification	'485 Claim 1
transistors that, when the second line of memory cells is selected for writing, couple the first power supply terminal to the first power supply line, decouple the first power terminal from the second line of memory cells, and couple the second power supply line to the first capacitance structure.	a second power supply line coupled to the second line of memory cells; and a switching circuit that has transistors that, connected between the first power supply terminal, the first power supply line, the second power supply line and the first capacitance structure wherein when the second line of memory cells is selected for writing, couple the first power supply terminal to the first power supply line, decouple the first power supply terminal from the second line of memory cells, and couple the second power supply line to the first capacitance structure.

VLSI Br. at 16 (citing '485 patent, 6:47-58); DX-31 [Apsel Suppl. Decl.] ¶ 12.

But as the Federal Circuit has expressly confirmed, merely "paraphrasing means-plus-function claim language in the specification alone does ***not*** describe any structure." *Tomita Techs. USA, LLC v. Nintendo Co.*, 594 F. App'x 657, 662 (Fed. Cir. 2014) (high-level diagram with a box labeled as "offset presetting means" merely paraphrased the claim language and thus did not describe any structure); *see also Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1364 (Fed. Cir. 2012) (recitation of "control device" in specification did not provide corresponding structure for "control means" because it did not provide any additional structure); *Hitachi Consumer Elecs. Co. v. Top Victory Elecs. (Taiwan) Co.*, 2012 WL 5494087, at *27 (E.D. Tex. Nov. 13, 2012) ("[T]he disclosure of 'video processor sections' in the Summary of the Invention merely repeats the language of the claim and therefore is not corresponding structure for purposes of 35 U.S.C. § 112 ¶ 6.").

As such, consistent with well-established Federal Circuit law, the Court should look to the specific structures that the '485 specification identifies for performing the claimed function—just as Intel has proposed. *Bennett Marine, Inc. v. Lenco Marine, Inc.*, 549 F. App'x 947, 954 (Fed.

Cir. 2013) (corresponding structure for a "control circuit" should be "limit[ed to] the control circuit portion of the corresponding structure … [of] the specific circuit shown in figure 2 and its equivalents," rather than "construed broadly" as a "generic circuit").

2. The Specification Supports Intel's Proposed Constructions.

a. Intel's proposed "first coupling means"

VLSI also attacks Intel's construction for the "first coupling means"—a transistor (52 or 96) and clamping circuit—as supposedly inconsistent with the specification. VLSI Br. at 16-19. But these attacks rest on incorrect assertions about how the claimed technology operates.

First, VLSI's argument that transistors 52 and 96 decouple the relevant components (rather than coupling them) confuses the role of these transistors during a write operation. VLSI Br. at 17-18. The specification discloses reducing the voltage supplied to a line of memory cells being written to by: (1) decoupling that line of memory cells from the power supply terminal; and (2) coupling that line of memory cells to the capacitance structure for charge sharing. DX-2 ['485 patent], 4:33-44, 6:16-27. The lines of memory cells that are ***not*** being written to remain coupled to the power supply terminal. *Id.*, 4:52-53 ("The supply voltage is ***only*** reduced on the ***columns being written to***."). In Figure 2, this "decoupling" function is performed, for example, by making transistor 52 non-conductive when writing to the memory cells in column 13 (the line of memory cells associated with transistor 52). *Id.*, 4:33-39, 6:17-22 (similar for Fig. 3). In contrast, transistor 52 remains conductive when writing to the memory cells in column 15. *Id.*, 4:52-53.

Further, claim 17 associates the "first coupling means" with a line of memory cells that is ***not*** being written to (the claimed first line of memory cells). This first line of memory cells remains ***coupled*** to the power supply terminal when another line of memory cells (the claimed second line of memory cells) is being written to. *Id.*, 10:7-9. This is exactly the function performed by the "first coupling means" structure that Intel has identified (transistor 52 and clamping circuit

46), when the claimed second line of memory cells is mapped to column 15 of Figure 2. When writing to the memory cells in column 15 (which correspond to the claimed ***second*** line of memory cells), transistor 52 couples the first power supply line for the memory cells in column 13 (corresponding to the claimed ***first*** line of memory cells) to the power supply terminal as specified by claim 17. DX-31 [Apsel Suppl. Decl.] ¶¶ 14-15. Thus, VLSI is wrong to contend that transistor 52 decouples (rather than couples) the power supply terminal and first power supply line when writing to the memory cells in column 15 (corresponding to the claimed second line of memory cells).

Second, VLSI's argument that the clamping circuit plays no role in the coupling ignores the patent's disclosure that the clamping circuit is part of the structure that "couples" the power supply terminal and first power supply line. DX-6 [Apsel Decl.] ¶¶ 79-82. That the clamping circuit also performs additional functions as well is legally irrelevant. *See Intellectual Prop. Dev., Inc. v. UA-Columbia Cablevision of Westchester, Inc.*, 336 F.3d 1308, 1320 & n.9 (Fed. Cir. 2003) (holding disclosed corresponding structure could perform multiple related functions). Here, the ability of the clamping circuit to perform the additional function that VLSI identifies—i.e., limiting the voltage drop on the power supply lines—results directly from the fact that the clamping circuit couples the power supply line to the power supply terminal. DX-31 [Apsel Supp. Decl.] ¶ 16.

Finally, although VLSI criticizes Intel for focusing on Figures 2 and 3 of the '485 patent, VLSI Br. at 16-17, those are the ***only*** embodiments that disclose corresponding structure. And VLSI's complaints about the reference numbers in Intel's construction are misplaced. Intel does not argue that these numbers affect the scope of the claim; instead, consistent with common practice, Intel included those numbers merely as a guide to the relevant structure disclosed in the specification. *E.g.*, *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1170 (Fed. Cir. 2015)

("[T]he structures corresponding to the claimed function … encompass only 'microprocessor ***23***' and 'memory unit ***24***.'"); *WhatsApp Inc. v. Intercarrier Commc'ns, LLC*, 2014 WL 5306078, at *10 (N.D. Cal. Oct. 16, 2014) (including reference numbers in corresponding structure).

b. Intel's proposed "second coupling means"

VLSI's challenges to Intel's proposed structure for the "second coupling means"—transistor 54 or 94—should also be rejected. VLSI Br. at 18-19. VLSI's reference to the specification's generic statement that, in other embodiments, these structures "can be different" is not disclosure of corresponding structure. *See Fonar Corp. v. Gen. Elec. Co.*, 107 F.3d 1543, 1551 (Fed. Cir. 1997) ("The '966 specification discloses use of a generic gradient wave form. Although it states that other wave forms may be used, it fails to specifically identify those wave forms.").

D. Disputed Term: "decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" (claim 17)

Intel's Construction	VLSI's Construction
Function: "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" **Structure**: None, indefinite	**Function**: "decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells" **Structure**: "a switching circuit, or equivalents thereof"

As Intel's opening brief demonstrated, the '485 specification does not disclose ***any*** structure for performing the claimed function of "decoupling the ***first power supply line*** from the ***second line of memory cells***." Intel Br. at 17-19. These two components are never coupled in the first place—it is therefore not surprising that there is no disclosed structure for ***decoupling*** them. The Court should reject VLSI's attempts to sidestep this lack of disclosed structure, which renders the claim indefinite.

First, the language VLSI relies on as purportedly disclosing a "switching circuit" for the

"decoupling" means is the ***same*** generic paragraph that it relies on for disclosing a "switching circuit" for the two "coupling" means. VLSI Br. at 20 (citing '485 patent, 6:47-58). As explained above, this paraphrasing of claim language "does ***not*** describe any structure." *Tomita Techs.*, 594 F. App'x at 662; *see Ergo Licensing*, 673 F.3d at 1364.

Second, even if the purported "embodiment" that VLSI identifies disclosed structure, it does ***not*** perform the claimed function of "decoupling the first power supply ***line*** from the second line of memory cells." Instead, VLSI quotes language referring to a "switching circuit" that "decouple[s] the first power ***terminal*** from the second line of memory cells." DX-2 ['485 patent], 6:47-58. As the specification confirms, the "first power terminal" and the "first power supply line" are distinct structures: the first power supply ***terminal*** is the voltage source (V_{DD}), whereas the first power supply ***line*** is the conductor (35 or 67) that carries the voltage to the first line of memory cells. *Id.*, 3:39-48, 5:22-28. This is shown, for example, in Figure 2:

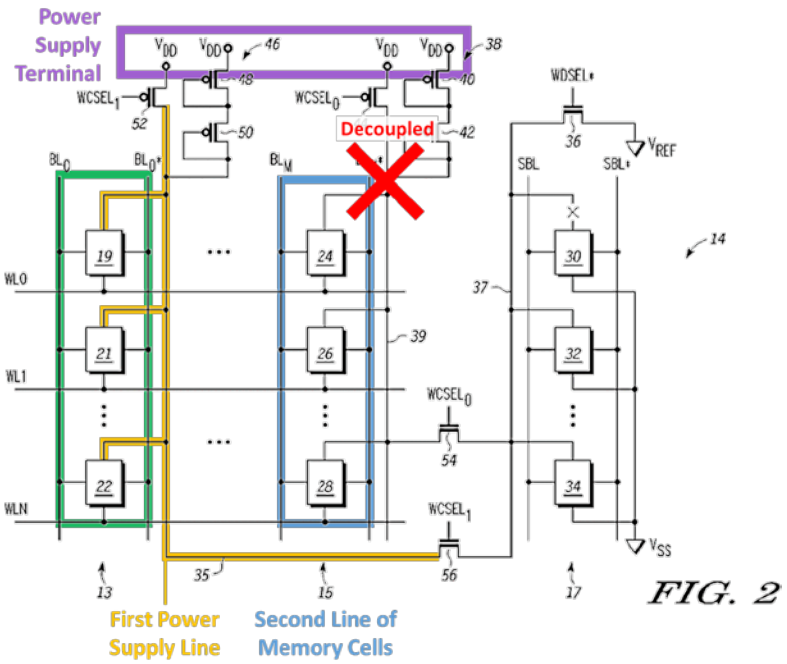

FIG. 2

Thus, the specification passage on which VLSI focuses describes ***no*** structure that performs the claimed function of "decoupling the first power supply ***line*** from the second line of memory cells."

In fact, it would be impossible for any "switching circuit" to decouple components that are never coupled in the first place.[8]

Finally, Dr. Conte's conclusory declaration citing the same two specification passages as VLSI's brief should not be accorded any weight. *Tomita Techs.*, 594 F. App'x at 662-63 ("[E]xpert testimony cannot gloss over the total absence of structure in the cited portion of the specification."). Like VLSI's brief, Dr. Conte fails to identify ***any*** corresponding structure in the specification that performs the claimed function of the "decoupling means" recited in claim 17.

IV. U.S. PATENT NO. 7,606,983

A. Disputed Term: "indication of a [the] specified order" (claims 1, 9, 11)

Intel's Construction	VLSI's Construction
"a second, different indication that indicates a | the specified order"	Plain and ordinary meaning

In its opening brief, Intel explained in detail why the "indication of a [the] specified order" limitation should be construed to require a ***second***, separate indication that is ***different*** from the first "indication" limitation—based on (1) the plain claim language, which sets forth two distinct "indication" requirements, one that depends on the other, and each of which must include different information; and (2) the prosecution history, in which the patentee confirmed Intel's plain meaning construction by distinguishing prior art on the basis that it only contained a single indication, while emphasizing the two-indication requirement of the claims at issue. Intel Br. at 20-23.

VLSI raises three arguments in response, none of which has merit.

[8] VLSI relies on a similar statement in the patent's abstract, VLSI Br. at 20, but that too simply paraphrases the claim language. It therefore cannot provide the necessary structure for the "decoupling" means. *Ergo Licensing*, 673 F.3d at 1364. This is particularly true given that, as described above, the specification discloses ***no*** structure for performing the claimed function.

First, VLSI maintains that no construction is necessary because the disputed limitation has an "***undisputed*** plain and ordinary meaning." VLSI Br. at 27. But in making that argument, VLSI never states what that supposed "undisputed" meaning could be—i.e., another improper attempt by VLSI to conceal its real position. *See NobelBiz,* 2015 WL 225223, at *13; *Datatreasury Corp.*, 2009 WL 1393068, at *65. VLSI also admits that a "disagreement between the parties" does exist, VLSI Br. at 27—which undermines VLSI's "undisputed" argument and confirms a need for the Court to construe this term. *See Eon Corp. IP Holdings v. Silver Spring Networks, Inc.*, 815 F.3d 1314, 1318-19 (Fed. Cir. 2016) (reversing "plain and ordinary meaning" instruction where parties "actively disputed" the term's meaning because "the court left this question of claim scope unanswered, leaving it for the jury to decide"); *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008) ("When the parties raise an actual dispute regarding the proper scope of these claims, the court, not the jury, must resolve that dispute.").

Second, VLSI asserts that requiring a "second" and "different" indication would impose "extra-textual constraints" and preclude "intermingl[ing] the two recited indications within a single data field." VLSI Br. at 27. But these "constraints" involving "two recited indications" come ***directly from the plain claim language***—which expressly requires two different "indications," each of which must convey different information, and with the second "indication" depending on the first "indication" (thus confirming they are two different things). Intel Br. at 21.

These are also the same "constraints" that the applicant relied on in defending the claims' validity during prosecution—during which (1) the Examiner relied on a ***single bit*** disclosed in the prior art as satisfying both "indication" limitations, and (2) the applicant successfully argued against and overcame those rejections by representing that the "***claimed invention***" requires "***two different*** indications." Intel Br. at 21-22. These arguments—made to secure allowance of the

claims—indisputably confirm that the plain claim language requires two different indications. It also helps explain why VLSI chose to ignore the prosecution history in its opening brief.

Further, even under VLSI's theory that the claim language in isolation can be read such that a ***single*** "indication" can meet ***both*** "indication" requirements (which it cannot, as discussed above), the applicant's statements during prosecution would alternatively constitute a clear and unmistakable disclaimer that precludes such a reading. Intel Br. at 23 n.2. *See, e.g.*, *Computer Docking Station*, 519 F.3d at 1374 ("[A] patentee may limit the meaning of a claim term by making a clear and unmistakable disavowal of scope during prosecution. A patentee could do so, for example, by clearly characterizing the invention in a way to try to overcome rejections based on prior art." (citation and internal quotation marks omitted)).

Finally, VLSI argues that Intel's construction would exclude "preferred embodiments" and does not cover any two-indication examples. VLSI Br. at 27. As an initial matter, the '983 patent does not describe any embodiments as "preferred."[9] And contrary to VLSI's suggestion, the patent ***includes*** embodiments that, consistent with Intel's construction, utilize ***two different*** indications. For example, the patent describes an embodiment where the two separate indications are thread ID signal 370 (a first indication of whether a request is to be performed in a sequential order) and sequence number signal 372 (a second indication of the specified order):

> In yet other embodiments, thread ID signal 370 may be used in conjunction with sequence-number signal 372. Requests having different thread ID values have no ordering constraint among them. Requests having the same thread ID values are to be performed in the increasing (or decreasing) numerical order of the sequence numbers.

[9] Rather, the specification discusses multiple embodiments, all of which include one or more "transaction ordering signals," and no embodiment is singled out as "preferred." DX-3 ['983 patent], 6:26-32, 6:38-7:29. In fact, the patent expressly states that "[t]he semantics of, and even the presence of each transaction-ordering signal, may vary among various embodiments of the invention." *Id.*, 6:32-34.

DX-3 ['983 patent], 6:48-53. Intel's construction covers this two-indication embodiment—which VLSI does not even discuss in its brief. DX-30 [Hagersten Suppl. Decl.] ¶ 6.

In contrast, many of the "single field" embodiments that VLSI cites are not covered by the asserted claims—even under VLSI's own reading. *Id.* For example, VLSI cites an embodiment in which only thread ID signal 370 is used and "multiple requests having the same thread ID value are to be performed in ***the order in which they are generated***, and there are ***no constraints*** among transactions having different thread IDs." *Id.* ¶ 7; DX-3 ['983 patent], 6:43-47. That embodiment does not satisfy the claims under VLSI's position because there is ***no indication of "specified order" in the access request*** (instead, the order is determined by when the processor generates the access request).[10] There is no need to construe the claims to capture this embodiment involving just a single indication. *See TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008) ("The mere fact that there is an alternative embodiment disclosed in the [patent] that is not encompassed by [our] claim construction does not outweigh the language of the claim, especially when the court's construction is supported by the intrinsic evidence.").

For these reasons, Intel's construction should be adopted because it correctly reflects the plain meaning scope of the claims—based on the claim language itself and prosecution history.

V. U.S. PATENT NO. 7,793,025

A. Disputed Term: "storage device for storing priority level information" (claims 1, 9) / "sets of priority levels in ... storage devices" (claim 17)

[10] In addition, two embodiments that use only sequence number signal 372 do not have an indication of the specified order. *Id.*, 7:3-7 ("In other embodiments, multiple requests having the same sequence number value may be performed ***in any order***. In other embodiments, multiple requests having the same sequence number value are to be performed in ***the order in which they are generated***."). And ***none*** of the embodiments using only last-in-thread signal 374 have an indication of the specified order. Instead, when this signal is used, it merely marks the beginning and end of an ordered sequence; it does not indicate the "specified order." *Id.*, 7:13-22; DX-30 [Hagersten Suppl. Decl.] ¶ 8.

Intel's Construction	VLSI's Construction
"hardware for storing priority level information that is not rewritten by software when the system changes mode or context" / "hardware for storing priority levels that are not rewritten by software when the system changes mode or context"	Plain and ordinary meaning

Intel previously explained in detail why the "storage devices" in these limitations should be construed to require hardware that is not rewritten by software when the system changes mode or context. Intel's construction is firmly grounded in the patentee's own clear statements in the patent and prosecution history that (1) repeatedly disparage and claim to improve upon software-based systems that rewrite interrupt priority values, and (2) instead describe as "the present invention" a hardware-based approach that does not use software to rewrite priority levels. Intel Br. at 25-31.

In its brief, VLSI admits for the first time that "storage devices" are "hardware for storing" information. VLSI Br. at 33 ("VLSI does not object to providing that a storage device is hardware for storing information …."). But it continues to incorrectly maintain that the claims encompass the very systems it disparaged and disclaimed—i.e., those that use software to rewrite interrupt priority values when the system changes mode or context.

First, VLSI wrongly accuses Intel of "attempting to narrow the claims by importing elements into them from selected embodiments in the specification." VLSI Br. at 34. As Intel's opening brief made clear, that construction comes ***directly*** from the patent and prosecution history, which (1) describe "the present invention" as a hardware-based approach, (2) criticize software-based approaches in the prior art, and (3) claim to improve over prior art software-based approaches in just one way: by using a hardware-based system that does not use software to rewrite the interrupt priority values when the system changes mode or context. Intel Br. at 26-31. VLSI cannot reverse these many unambiguous representations of claim scope based on unfounded

assertions that Intel is trying to limit the claims to certain embodiments.

Second, VLSI argues that Intel's construction is improper because it would exclude "some embodiments in which updates may occur under software control." VLSI Br. at 34. But there is no such embodiment. VLSI points only to a statement in the patent that "[b]y implementing the interrupt priority register 212 as a read/write register, the assigned priority values may be updated or changed under software control." VLSI Br. at 34 (quoting '025 patent, 6:60-63). But the very next sentence—which VLSI leaves out—***teaches against doing so***, followed by a prescription for using hardware instead:

> By implementing the interrupt priority register 212 as a read/write register, the assigned priority values may be updated or changed under software control. ***However***, there is a latency ***penalty***, as well as processor ***overhead***, ***associated with having frequent software updates of the interrupt settings***. To enable changes in the assignment of interrupt priority levels to pending interrupts, selected embodiments of the present invention ***provide a plurality of interrupt priority registers*** [i.e., hardware] for use with different system modes or contexts that require alternate priorities.

DX-4 ['025 patent], 6:60-7:3. In other words, this passage simply affirms that, because of the prior art problems associated with updating interrupt priority registers via software, the ***claimed invention*** requires switching between hardware devices when the system mode changes, rather than using software to rewrite the priorities—just as Intel has proposed. Accordingly, despite VLSI's claims to the contrary, there is no software-based embodiment of the alleged invention that Intel's construction would exclude.[11]

[11] It makes sense that, even though the claimed invention does not use software to change priority levels, the interrupt priority registers would consist of read/write registers that can ***initially*** be written by software. For example, when a system built in accordance with the claimed invention first boots up, it may initialize the interrupt priority registers with priority values. Accordingly, Intel's proposed construction does not require that the interrupt priority registers are ***never*** written by software; instead, it requires that the priority level information stored in the registers is not "***re***written by software ***when the system changes mode or context***."

Third, VLSI argues that Intel's construction "omits the 'one or more' language that appears in claim 17" and "seeks to replace [that term] with 'a plurality.'" VLSI Br. at 35. But the language from claim 17 that Intel proposed for construction is "sets of priority levels in ... storage devices," not "sets of priority levels in ***one or more*** storage devices." Thus, it is not Intel's intention to replace or define the "one or more" language; nor does Intel contend that the claim requires a "plurality" ***of hardware devices***. Intel's construction simply provides a definition for the language adjacent to "one or more" (i.e., "sets of priority levels in ... storage devices"), thereby clarifying that it requires hardware for storing priority levels that are not rewritten by software when the system changes mode or context.

Finally, VLSI misleadingly maintains that Intel's construction must be wrong because it supposedly requires "storing the hardware itself" (rather than data). VLSI Br. at 35-36. That obviously is not Intel's intention. Rather, Intel's construction merely requires that (1) the "storage devices" of claim 17 are hardware—which as noted above, VLSI now admittedly does not dispute, and (2) the priority level information ***stored in*** those hardware devices is not rewritten by software when the system changes mode or context. Intel has never argued that its construction would require storing "the hardware itself."[12]

VLSI also faults Intel for "giving almost exactly the same meaning to two materially different terms" ("storage device for storing priority level information" as used in claims 1 and 9 and "sets of priority levels in … storage devices" as used in claim 17). VLSI Br. at 36. But Intel's construction already accounts for any such differences. Both claims require priorities ("priority

[12] Intel could, but does not believe it is necessary to, alter its construction grammatically (without altering the construction's substance) to address VLSI's complaints about the construction's overall grammatic effect when inserted verbatim into the claim. Nevertheless, to the extent the Court believes that type of modification would be helpful, Intel would not oppose doing so.

level information" in claims 1 and 9, and "sets of priority levels" in claim 17) to be stored in hardware devices (i.e., "storage devices" in all three claims). Intel's construction does not vary the "priority level information" in claims 1 and 9 or the "sets of priority levels" in claim 17. Instead, as explained above, Intel's construction merely clarifies—based on representations by the '025 patentee—that this information is stored in hardware devices and is not rewritten by software when the system changes mode or context.

In the end, VLSI's predecessor-in-interest represented in its patent and to the Patent Office that the claims have the limited scope embodied by Intel's proposed construction, and those representations are binding on VLSI here. *See CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d 1146, 1158 (Fed. Cir. 1997) ("[T]hrough statements made during prosecution … an applicant … may commit to a particular meaning for a patent term, which meaning is then binding in litigation.").

B. Disputed Term: "priority level information associated with a [first/second] system mode for each of the one or more interrupt requests" (claim 1) / "priority level information associated with a [first/second] system mode" (claim 9)

Intel's Construction	VLSI's Construction
"priority level information associated with a [first/second] system mode for each of the one or more potential interrupt requests"	Plain and ordinary meaning

Intel's opening brief explained why the limitations in claims 1 and 9 directed to mode-specific "priority level information" should be construed to require priority level information for ***each potential*** interrupt request (rather than just for pending interrupt requests that actually occur)—in light of the express representations about the narrow scope of these limitations that the patentee made in the '025 patent itself, and again during prosecution to overcome prior art rejections. Intel Br. at 31-33. None of VLSI's arguments changes that result.

First, VLSI asserts that Intel is "changing the plain language of the claims" by proposing

to add the word "potential" before "interrupt requests." VLSI Br. at 30-31. But as Intel explained in its opening brief, it was ***the patentee*** who supplied that meaning—(1) by explaining over and over in the patent that "interrupt priority registers" (the hardware devices of claims 1 and 9) must store priority information for each ***potential*** interrupt request that might be received, and (2) by overcoming prior art rejections for claims 1 and 9 during prosecution only after representing that those limitations require storing priority level information for each ***potential*** interrupt request. Intel Br. at 31-33. VLSI completely ignores this intrinsic evidence and resulting disclaimer, which alone requires Intel's construction.[13]

VLSI relatedly argues that Intel's construction cannot be correct because claims 17 and 20 contain the words "potential interrupt request," while claims 1 and 9 just refer to an "interrupt request." But as Intel already explained, the patent owner argued during prosecution—again to overcome prior art rejections—that ***every claim*** requires storing "each of the ***potential*** pending interrupt requests." Intel Br. at 32-33 (explaining how, for claims 1 and 9, the applicant distinguished prior art by arguing that "[a]s described in the Application, the interrupt priority registers are provided for storing values corresponding to each of the ***potential*** pending interrupt requests"). The law requires binding VLSI to the same claim scope that the patentee previously represented to secure issuance of the claims. *See CVI/Beta Ventures*, 112 F.3d at 1158; *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("The prosecution history limits the

[13] VLSI suggests that the file history supports its position. VLSI Br. at 31-32. But its citations to the file history, if anything, support Intel's position. These quotations—which reference both the limitation of claim 1 at issue here ("each of the one or more interrupt requests") and the similar limitation in claim 17 ("each potential pending interrupt request")—are followed by arguments from the applicant, regarding ***both*** limitations, about interrupt priority storage devices storing "priority values corresponding to each of the potential pending interrupt requests." DX-16 [Response] at 7 (underlining in original). Thus, the applicant effectively argued that there is no difference between these limitations, in spite of claim 17's inclusion of the word "potential."

interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution.").

Second, VLSI argues that claims 1 and 9 cannot be limited to "potential interrupt requests" because the patent purportedly mentions four other types of "interrupt requests." VLSI Br. at 30 (discussing "masked interrupt requests," "received interrupt requests," "actual pending interrupts," and "handled interrupt requests"). But the claim language at issue requires storing the claimed "priority level information" in "***interrupt priority storage devices***." And the ***only*** type of interrupt information that the patent describes as stored in "interrupt priority registers" (i.e., the "interrupt priority storage devices" of claims 1 and 9) is priority level information for ***potential*** interrupt requests:

- "One or more ***interrupt priority registers*** are also provided for storing priority values corresponding to each of the ***potential*** pending interrupt requests …." DX-4 ['025 patent], 2:64-67.
- "[T]he ***interrupt priority register 212*** may store predetermined priority values for each of the ***potential*** interrupts …." *Id.*, 5:65-67.
- "The ***interrupt priority register 212*** may be implemented using any desired storage mechanism to store an interrupt value ***for each potential interrupt*** …." *Id.*, 6:3-6.
- "[O]ne or more ***storage devices*** are provided for ***storing a plurality of sets of priority levels***, where each set of priority levels is associated with a different system mode and specifies a priority level ***for each potential pending interrupt request***. In the ***storage device(s)***, … each multi-bit priority level indication is assigned to a corresponding ***potential*** pending interrupt request." *Id.*, 10:51-61.
- "Each entry in each ***interrupt priority register*** corresponds to a ***possible*** pending interrupt

request …." *Id.*, 3:3-5.

By contrast, the patent never suggests that interrupt priority registers store priority level information for any ***other*** types of interrupts. The specification instead explains that other types of interrupts, and data related to those interrupts, are stored in ***other types*** of registers:

- "***Pending*** interrupt requests" are stored in an "***interrupt pending register***." *E.g.*, *id.*, 2:52-54 ("[A] plurality of pending interrupt signals … may be stored in an interrupt pending register …."); *id.*, 2:62-63 ("[P]ending interrupt requests … may be stored in an interrupt pending register."); *id.*, 6:9-12 (discussing "selection of pending requests from the interrupt pending register 210"); *id.*, Fig. 3 (showing "pending registers" 310 as distinct from "interrupt priority registers" 321 and 322).
- What VLSI calls "***received*** interrupt requests"—i.e., "requests that have reached the processor," VLSI Br. at 30—are stored in an "***interrupt source register***." DX-4 ['025 patent], 1:40-44; Dkt. 81-1 [Conte Decl.] ¶ 45.c (VLSI's expert admitting that "[t]he interrupt source register 204 selectively stores all interrupt requests received via the physical conductors or from on-chip sources …." (quoting '025 patent, 4:65-5:3)).
- Data used to "mask" (i.e., enable or disable) interrupts is stored in an "***interrupt enable register***," and once an interrupt has been "masked," if it is enabled, it becomes a ***pending*** interrupt that is stored in the "***interrupt pending register***" (as noted above). Dkt. 81-1 [Conte Decl.] ¶ 45.b ("By logically combining (e.g., with a logical AND gate) the individual bits of the interrupt source register and the content of the ***interrupt enable register***, the interrupt requests may be effectively ***masked*** and stored in an ***interrupt***

pending register." (quoting '025 patent, 1:46-50)).[14]

Because none of these other types of interrupt requests use an "interrupt priority register," as claims 1 and 9 require, the discussion of them is irrelevant for purposes of this claim construction dispute.

That the '025 patent universally describes the claimed interrupt priority registers as storing the claimed interrupt priority levels for each potential interrupt request is not surprising; this feature is central to the operation of the claimed invention. By storing predetermined interrupt priority levels for ***potential*** incoming interrupts, the system is ready to assign priorities to the ***actual*** pending interrupts upon their arrival. *E.g.*, DX-4 ['025 patent], 5:65-6:18 ("[T]he interrupt priority register 212 may store ***predetermined*** priority values for each of the ***potential*** interrupts …. To assist with the selection of pending requests from the interrupt pending register 210, the priority values are stored in an interrupt priority register 212 …, such that the interrupt priority register 212 can be read to determine which priority values are assigned to each pending interrupt ….'). Indeed, the very nature of the '025 system is to predetermine—and store in hardware—the priorities of potential interrupts for possible system modes or contexts before those priorities are used to assign priorities to incoming interrupt requests. These predetermined priority levels provide the purported benefit of the invention. *Id.*, 2:5-11 ("[I]nterrupt priority levels have conventionally been controlled by ***software***, which means that any changes in the prioritization of interrupts (which can occur when the system changes mode or context) requires ***additional time*** and programming complexity to switch the prioritization ***by re-writing the interrupt priority registers*** ….").

[14] VLSI contrives another type of interrupt request called "handled interrupt requests"—i.e., according to VLSI, "requests that have been received and acted upon." VLSI Br. at 30. The '025 patent does not use that term, but interrupts that have been "handled" are, under VLSI's definition, not stored anywhere because they have already been processed. DX-4 ['025 patent], 8:37-47.

Third, VLSI argues that Intel's construction would improperly exclude an embodiment described in Figure 4, which VLSI characterizes as involving interrupt priority registers that store only priorities for ***actual*** pending interrupts. VLSI Br. at 32. But that is not what Figure 4 or its related description teaches. Rather, as detailed below, the steps of the method shown in Figure 4 are entirely consistent with Intel's construction:

- At step 402, the method "receive[s] (masked) interrupt signals," DX-4 ['025 patent], Fig. 4, in which "[a] first storage device (e.g., an interrupt source register or interrupt pending register) having a plurality of inputs is provided," *id.*, 9:19-26, and the ***pending*** registers (item 210 in Fig. 2 and item 310 in Fig. 3) are described as storing the ***pending*** interrupts, *id.*, 5:40-46.
- At step 403, "interrupt priority storage devices (e.g., interrupt priority registers) are provided" that store different context-based priority levels. *Id.*, 9:24-26. These interrupt priority registers (item 212 in Fig. 2 and items 321 and 322 in Fig. 3) store "predetermined" priority values for "each ***potential*** interrupt." *E.g.*, *id.*, 5:65-6:9, 7:51-61.
- In step 404, a mode-specific interrupt priority register provides priority values for potential pending interrupts that are appropriate for the system mode. *Id.*, 9:42-54.
- Finally, in step 405, these priority values are used to assign priorities to the ***actual pending*** interrupts. *Id.*, 9:54-57 ("[T]he logic circuitry prioritizes the interrupt signals and provides an interrupt request signal which will cause an interrupt to occur in the data processing system ….").

As such, Figure 4 is not directed to an embodiment in which interrupt priority registers store only priorities for actual pending interrupts, despite VLSI's claim to the contrary.

C. Disputed Term: "providing a plurality of interrupt priority storage devices … and providing a plurality of interrupt priority storage devices …" (claim 1)

Intel's Construction	VLSI's Construction
Indefinite	Definite

Claim 1 of the '025 patent includes the following two "providing" limitations (with differences underlined):

First "providing" limitation	Second "providing" limitation
providing ***a plurality*** of interrupt priority storage devices comprising a ***first*** interrupt priority storage device for storing priority level information associated with a first system mode, and a ***second*** interrupt priority storage device for storing priority level information associated with a second system mode; and	providing ***a plurality*** of interrupt priority storage devices comprising a ***first*** interrupt priority storage device for storing priority level information associated with a first system mode <u>for each of the one or more interrupt requests</u>, and a ***second*** interrupt priority storage device for storing priority level information associated with a second system mode <u>for each of the one or more interrupt requests</u>; and

As explained in Intel's opening brief, this language is hopelessly indefinite—because it is unclear if the claim requires two priority storage devices and one plurality (if the "first" and "second" devices in both limitations refer to the same devices), or four devices altogether and two separate "pluralities" (if they refer to different devices). Moreover, if read to require four devices and two different pluralities of storage devices, the claim has insurmountable antecedent basis problems because it would be impossible to determine the antecedent basis for "***the*** plurality of interrupt priority storage devices" requirement appearing in the last limitation. Intel Br. at 34-35.

In its brief, VLSI contends that the scope of these limitations is unambiguous. But it does so by unilaterally picking one of two equally plausible ways to read the claim (as requiring only ***two*** priority storage devices and one plurality), and dismissing the other reasonable reading (as requiring ***four*** priority storage devices and two pluralities). VLSI Br. at 37-39. But even then, VLSI simply posits that one of ordinary skill "would understand that the overlapping, identically

phrased portions of the two elements ***could*** be satisfied by the same structures." *Id.* at 37. That is precisely the point. One of skill "could" read the claim that way, but also "could" read the same claim to require two different sets of structures—and VLSI does not argue otherwise. Thus, the claim should be found indefinite for this reason alone.

In support of its selective reading, VLSI asks the Court to disregard the overlapping portions of the second "providing" limitation as duplicative. But acceptance of that argument would violate the fundamental canon of claim construction that limitations should not be construed in a way that renders them superfluous. *See Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."). VLSI improperly seeks to render large portions of claim 1 redundant and meaningless because there is an incoherent contradiction in the way the claim is drafted, and that problem cannot be cured via claim construction.

VLSI suggests that its selective reading is required because the "providing" limitations in claim 1 do not refer to "first" and "second" ***pluralities*** of interrupt priority storage devices. VLSI Br. at 38. But VLSI cites no authority for the proposition that claims cannot be read to require separate structures unless they use such express terms—because that is not the law.

Nor can VLSI untangle the indefinite scope of claim 1 simply because the specification discloses an embodiment involving just two interrupt priority storage devices. *Id.* Indeed, as VLSI explains elsewhere in its brief, it would be improper to construe claim 1 by importing such an embodiment from the specification. As noted above, the plain language of claim 1 could just as equally be read as requiring four different interrupt priority storage devices—two of which would need to meet the requirements of the first "providing" limitation, and the other two that would need to meet the different requirements of the second "providing" limitation—and nothing in the

specification precludes that possibility.

VI. U.S. PATENT NO. 7,523,373

A. Disputed Term: "means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage" (claim 14)

Intel's Construction	VLSI's Construction
Indefinite	**Function**: "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage" **Structure**: "power supply selector, charge pump, scalable voltage regulator, or equivalents thereof"

Intel's opening brief detailed how the "means for providing" limitation of claim 14 is a means-plus-function term governed by 35 U.S.C. § 112, ¶ 6, and how the term is indefinite for two independent reasons: (1) the claim recites a nonsensical function that purports to require a ***second source*** to provide ***the same*** "operating voltage" to ***the same*** "memory" that another claimed structure already must supply; and (2) in any event, the '373 specification does not disclose any such second source structure that performs this nonsencial function. Intel Br. at 36-40.

VLSI asserts several arguments in response, each of which should be rejected.

First, VLSI argues that Intel has waived its indefiniteness argument for claim 14 by failing to assert it in its preliminary invalidity contentions (served in September 2019). VLSI Br. at 22. But VLSI failed to provide ***any*** preliminary infringement contentions for claim 14—and then waited until ***two weeks after*** Intel's deadline for invalidity contentions, and just shortly before Intel's opening brief was due in these *Markman* proceedings, to provide an infringement theory for claim 14 ***for the first time***. As such, VLSI has no basis to contend that Intel waived its

indefiniteness arguments by failing to raise those arguments sooner.[15]

Second, VLSI alleges that the claimed function for this means-plus-function term requires "providing ***the operating voltage*** to ***the memory***." VLSI Br. at 21. Yet, VLSI makes no effort to even attempt to explain how that function could be definite given that, as shown below and detailed in Intel's opening brief, claim 9 (from which claim 14 depends) already requires a separate structure (a "power supply selector") to perform the same function of supplying "***the operating voltage***" to "***the memory***":

Independent Claim 9	Dependent Claim 14 Requires
"***a power supply selector*** that supplies the first regulated voltage as ***the operating voltage of the memory***"	"The ***memory*** of claim 9, ***further*** comprising: … ***means*** for providing ***the operating voltage to the memory***"

Intel Br. at 36-37. *See Trustees of Columbia Univ. in City of N.Y. v. Symantec Corp.*, 811 F.3d 1359, 1367 (Fed. Cir. 2016) ("The claims are nonsensical in the way a claim to extracting orange juice from apples would be, and are thus indefinite.").[16]

Third, with respect to corresponding structure, VLSI argues that claim 14 is not indefinite because "the specification clearly links each of three separate structures to the recited function."

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[15] VLSI filed a motion to amend its infringement contentions on November 6, 2019. Dkt. 83. Although VLSI had not yet done so when it proposed this term for construction, or by the time the parties filed opening briefs, in an effort to avoid burdening the Court with potential multiple rounds of claim construction proceedings, Intel has briefed its claim 14-related arguments pursuant to the pre-existing claim construction schedule.

[16] In the '373 application, claim 9 (originally claim 11) did not require a "power supply selector" or any other structure for providing "the operating voltage" to "the memory"; these structural features instead appeared only in dependent claim 14 (originally claim 18). DX-32 ['373 Application] at 20-22 (showing claims 11 and 14); DX-33 [Issue Classification] at 1 (renumbering claim 11 to claim 9 and claim 18 to claim 14). During prosecution, however, the applicant ***added*** the "power supply selector" limitation to claim 9 (then claim 11), but did not make any corresponding changes to the already-existing structural requirements of claim 14 (then claim 18). DX-34 [Amendment] at 3-5 (showing amendment to claim 11, and no amendment to claim 18). Because this amendment to claim 9 introduced a fundamental inconsistency between independent claim 9 and dependent claim 14, claim 14 is indefinite.

VLSI Br. at 21-22 (identifying a "power supply selector," "scalable voltage regulator," and "charge pump" as the "three separate structures"). But claim 14 expressly provides that the "means for providing" (1) must be located ***within*** the claimed memory ("The memory of claim 9, further comprising: … means for providing"), and (2) must "provid[e] the operating voltage to the memory." None of the three identified components meets both requirements.

For example, VLSI relies on Figure 1 to argue that the specification discloses that the power supply selector performs the stated function. VLSI Br. at 22-24. And as illustrated below, Figure 1 shows power supply selector 21 (in green) located ***within*** memory 18 (in blue):

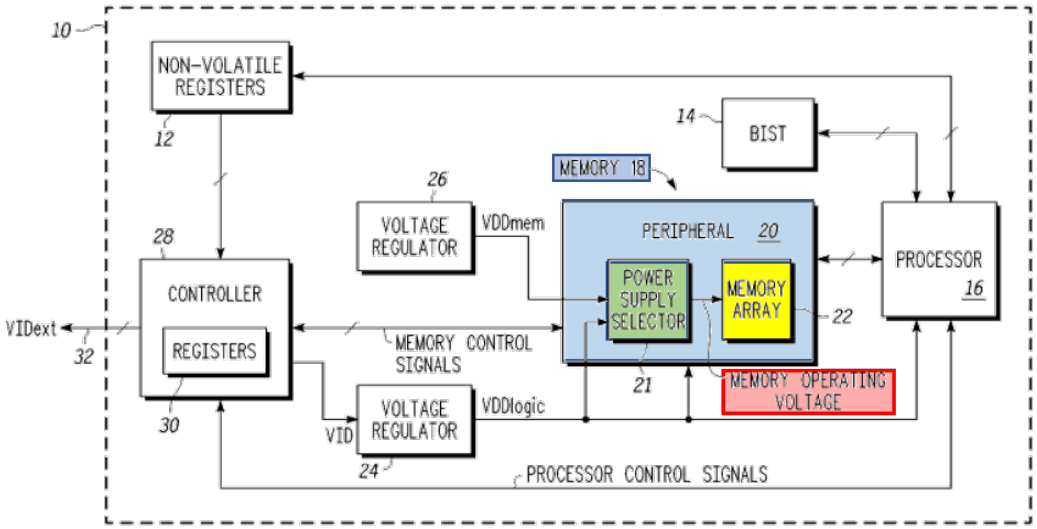

FIG. 1

DX-5 ['373 patent], Fig. 1. But as VLSI admits, in that embodiment, power supply selector 21 supplies the selected "memory operating voltage" (in red) to ***another component located in the same memory***: i.e., to memory array 22 (in yelow). VLSI Br. at 22 ("Both voltages are provided to a power supply selector, which, as seen in Figure 1, in turn ***provides a voltage level to memory array 22***."). Because when located ***within*** memory 18, the power supply selector does not provide

a voltage "***to*** the memory," it is not clearly linked to the VLSI's proposed claimed function.[17]

The '373 specification also discloses alternative embodiments in which a power supply selector may be ***external*** to memory 18. DX-5 ['373 patent], 2:58-59. Such an external power supply selector ***could*** provide an operating voltage "to the memory." But even in that case, the external power supply selector would not satisfy claim 14's other requirement for the "means for providing" to be ***within*** the memory. Moreover, VLSI cites no disclosed embodiment in which two different components—the power supply selector of claim 9 ***and*** the separate supplying structure required by claim 14—***both*** provide "***the*** operating voltage of ***the*** memory" to ***the*** memory. That is because there is no such embodiment. Intel Br. at 37-38.

VLSI argues that the corresponding structure may alternatively be a scalable voltage regulator or a charge pump. VLSI Br. at 26. For the scalable voltage regulator, VLSI relies only on the disclosures in column 8 of the patent. *Id.* (citing '373 patent, 8:16-44). But column 8 describes a scalable voltage regulator that provides a voltage ***to the logic***, VDDlogic—not the claimed voltage provided "to the memory," VDDmem. DX-5 ['373 patent], 8:42-44 ("Therefore, controller 28 may adjust VID accordingly to prevent regulator 24 [which outputs VDDlogic] from outputting the desired voltage selected by the selected state signal."). And importantly, claim 9 already requires a power supply selector—not a scalable voltage regulator—to provide the operating voltage to the memory. The patent is devoid of any embodiment where ***both*** a scalable

[17] VLSI misleadingly states that "the '373 Patent teaches that a power supply selector 'receives VDDmem and VDDlogic and ***provides*** one of these to [a memory] as the memory operating voltage." VLSI Br. at 22 (emphasis and brackets in original). Nothing in that partially-quoted passage, or elsewhere in the specification, refers to power supply selector 21 in Figure 1 as providing the operating voltage "to a memory," as VLSI's brackets suggest. Rather, the full quote merely states that the power supply selector is located in memory 18 and provides either VDDmem or VDDlogic to memory array 22, also within the memory. DX-5 ['373 patent], 2:52-55 ("***Memory 18 also includes a power supply selector 21*** which receives VDDmem and VDDlogic and ***provides one of these <u>to memory array 22</u>*** as the memory operating voltage.").

voltage regulator ***and*** a power supply selector provide ***the*** operating voltage to ***the*** memory. VDDlogic is merely an input to the power supply selector. *Id.*, 2:52-53 ("[P]ower supply selector 21 … receives VDDmem and VDDlogic ….").

Likewise, the patent does not disclose a charge pump that both (1) is located in the memory, and (2) provides the operating voltage to the memory. In support of this alleged structure, VLSI points to column 5, lines 54-61. VLSI Br. at 26. But that disclosure says only that "VDDlogic may be boosted during reads through the use of a charge pump." DX-5 ['373 patent], 5:59-60. It does not describe a charge pump that is ***within*** the memory, and that provides an operating voltage ***to the memory*** (including alongside a ***separate*** power supply selector, also supplying the memory with its operating voltage, as claim 9 further requires).

Finally, for the portion of VLSI's claimed function directed to "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage ***in response to the operating value selected by the processor being below the minimum operating voltage***," VLSI points to the embodiment described in column 8 of the patent. VLSI Br. at 25. But column 8 does not disclose a processor that selects an operating value for the operating voltage of the memory, as claim 14 requires. Instead, the only action taken by the processor in that embodiment is to select a "state"—not an "operating value." DX-5 ['373 patent], 8:21-23 ("Controller 28 may provide a selected state signal to select a DVFS state (where controller 28 may provide this signal ***based on a state selected by processor 16***).").

Instead of the processor, the '373 patent describes how a component within controller 28 (i.e., voltage selector 42) selects the operating value of the memory's operating voltage by using a state signal, provided by controller 28 based on the state selected by the processor, to look up the "selected voltage value" "(i.e., the desired voltage value for VDDlogic)." *Id.*, 8:26-29, 8:35-36.

Then, yet another set of components within controller 28 (comparator and override 44) determine whether the selected voltage value for VDDlogic is above the minimum operating voltage of the memory and, if not, sends a signal "to power supply selector 21 … to select VDDmem rather than VDDlogic to provide as the memory operating voltage to memory array 22." *Id.*, 8:55-58. Because column 8 does not disclose a processor that selects the operating value for the memory's operating voltage, none of VLSI's proposed structures performs the portion of VLSI's proposed function requiring "providing the operating voltage to the memory … in response to the operating value ***selected by the processor being below the minimum operating voltage***."

In sum, because VLSI has failed to identify ***any*** structure that the specification identifies as both (1) located within "the memory," and (2) performing VLSI's claimed function of "providing an operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage," the limitation should be found indefinite. *See Williamson*, 792 F.3d at 1352 ("If the patentee fails to disclose adequate corresponding structure, the claim is indefinite.").

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via the Court's CM/ECF system per Local Civil Rule CV-5(b)(1) on November 18, 2019.

/s/ J. Stephen Ravel
J. Stephen Ravel